

**DITF Toolkit****Substrates****Common Substrate Materials**

- |                                 |                     |                                      |
|---------------------------------|---------------------|--------------------------------------|
| • Alumina (99.5% min)           | $\epsilon_r = 9.9$  | $\text{Tan } d = 1.5 \times 10^{-4}$ |
| • Aluminum Nitride (K170)       | $\epsilon_r = 8.9$  | $\text{Tan } d = 2.0 \times 10^{-3}$ |
| • Beryllia (99.5%)              | $\epsilon_r = 6.7$  | $\text{Tan } d = 3.0 \times 10^{-3}$ |
| • Quartz                        | $\epsilon_r = 3.8$  | $\text{Tan } d = 3.0 \times 10^{-4}$ |
| • Sapphire (Perpendicular to C) | $\epsilon_r = 9.4$  | $\text{Tan } d = 1.0 \times 10^{-4}$ |
| • Sapphire (Parallel to C)      | $\epsilon_r = 11.5$ | $\text{Tan } d = 1.0 \times 10^{-4}$ |

**Standard Substrate Sizes** *(selected at the factory for optimum process)*

- |                              |   |
|------------------------------|---|
| • Alumina & Aluminum Nitride | 3.75" x 4.50", 3" x 3", 2.25" x 2.25, 1.00" X 1.00" |
| • Beryllia                   | 4" x 4", 3.75" x 4.50", 3" x 3", 2" x 2"            |
| • Quartz / Sapphire          | 3" x 3", 2.35" x 2.25", 2" x 2", 1" x 1"            |

**Metal Systems****NiCr / TaN Resistors****TiW (Pd,Ni) Au Sputtered Contacts**

- Fine Line Structures, <.0015" (38.1 $\mu$ )
- Cross-over Bridge Circuits
- Eutectic Die Attach

**Cu, Ni, Au Plated Contacts**

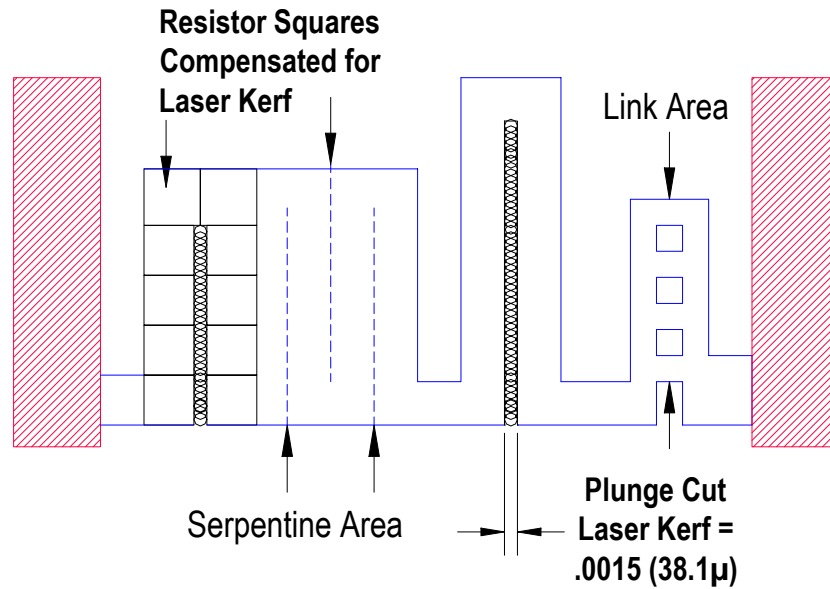
- High Power Requirements
- High Speed, Low Loss Conductors
- Nickel Oxide Solder Masks

**Metal System Properties**

Conductor	Thickness ( $\mu\text{m}/\text{mils}$ )	Line Resolution	Typical Sheet Resistance	At Spec. Thkns ( $\mu\text{m}/\text{mils}$ )	T.C. W/m $^{\circ}$ C)
Cu	5 / .197	.002"	2.5mW/sq.	38 / 1.49	393
Cu (Thick Option)	75 / 2.95	.004"	0.2mW/sq.	200 / 7.87	393
Ni	1.2 / .047	-	60mW/sq.	30 / 1.18	----
Au	3 / .118	-	7mW/sq.	30 / 1.18	299

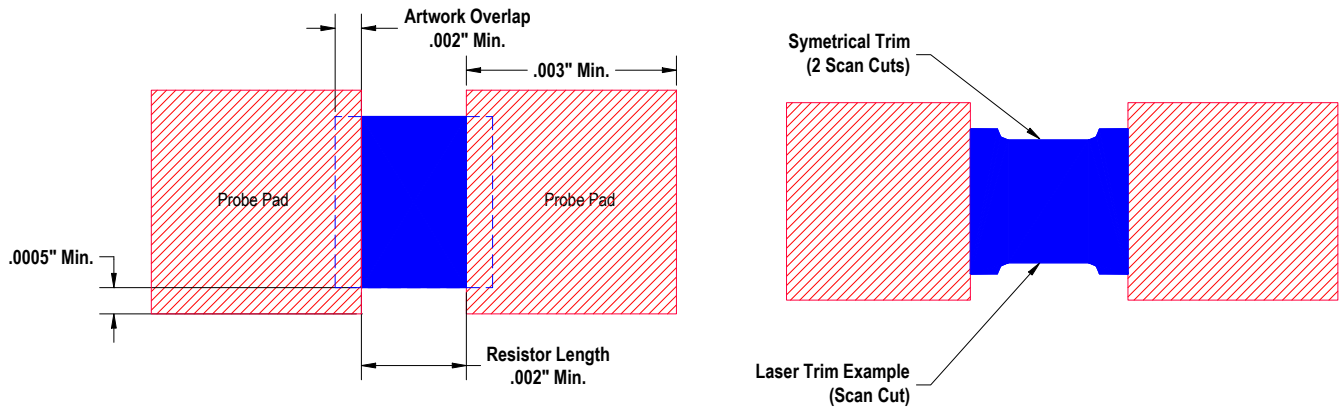
**Resistors**

Resistor Properties, 99.6% Alumina					
Material	TCR (ppm/°C)	Standard Sheet Resistivity ( $\Omega/\square$ )	Passivation	Stability	Tolerance
TaN	-125±25	10-125	Self Passiv.	<0.5%	1-10%
NiCr	0±25	10-250	Various	<0.2%	1-10%
Resistor Parameters for Additional Substrates					
Substrate Material	Standard Sheet Resistivity ( $\Omega/\square$ ) TaN / NiCr	Optional Sheet Resistivity ( $\Omega/\square$ )	TaN	NiCr	Comments
Beryllia	25-120 / 50 - 250	Check Factory	Yes	Yes	Laser trimmable to 1%. Design to allow up to 50% width reduction.
Aluminum Nitride	25-120 / 50 - 250	Check Factory	Yes	Yes	Laser trimmable to 1%. Design to allow up to 50% width reduction (scan cut).
Quartz	25-200 / 50 - 350	Check Factory	Yes	Yes	Design Dependant.
Sapphire	25-200 / 50 - 350	Check Factory	Yes	Yes	Design Dependant.



## Probe Pad and Artwork Overlap Requirements

*\*All resistors should be designed at value and final sheet resistivity needs to be stated clearly on drawing.*

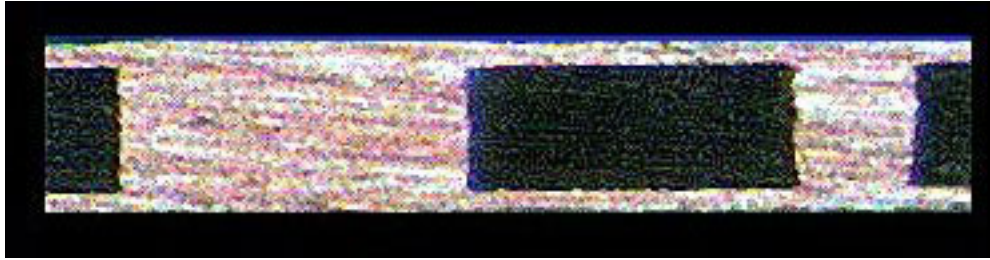


## Via Holes, Plated and Filled

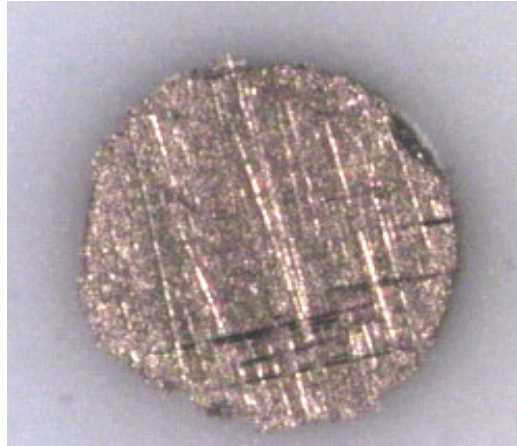
- Filled Via Material – Au or Cu
- Thermal Conductivity – Au=300 W/mK, Cu=393 W/mK
- Minimum Plated Via Diameter - .8/1 Aspect Ratio (*dia:ceramic thickness,  $\geq .007$ "*)
- Minimum Filled Via Diameter - .6/1 Aspect Ratio (*dia:ceramic thickness,  $\geq .007$ "*)



*Au Filled Vias in Ceramic Cross Section*

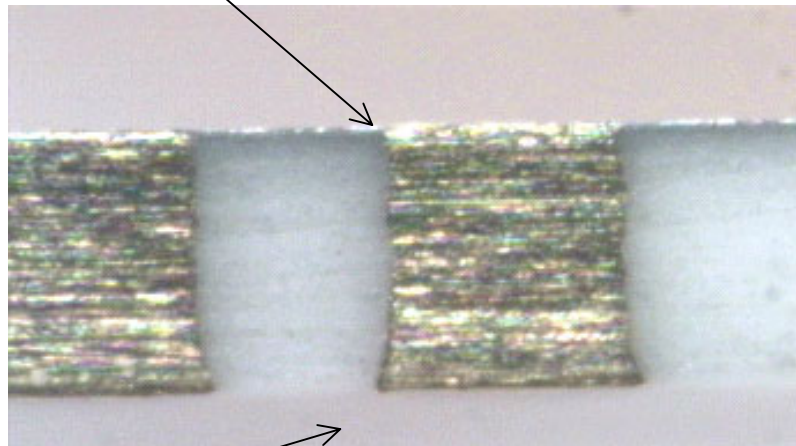


*Cross Section – Cu Vias and Metallization  
Glass Substrate for Illustration Purposes Only*



*Cu Filled Via*

*“A” – Circuit Side*

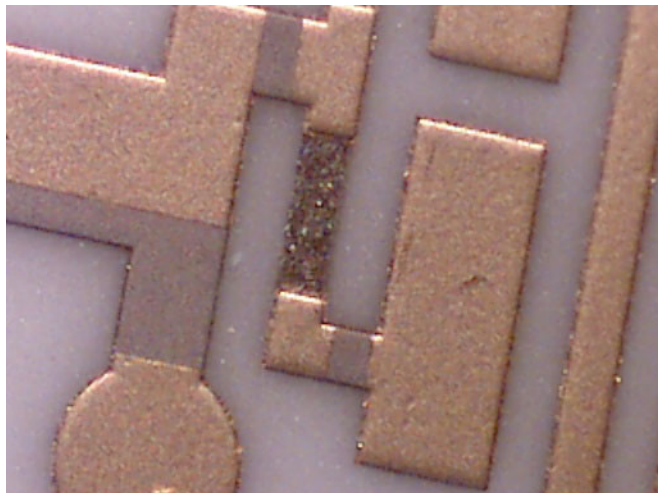
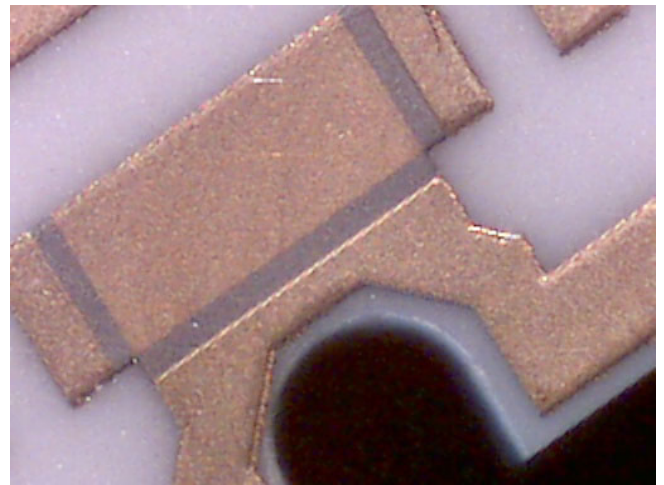


*“B” – Back Side* — *Filled Via Cross Section*

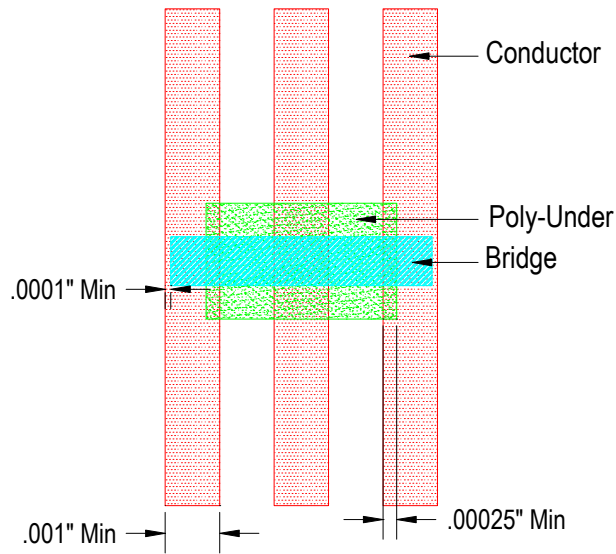
- Minimum Capture Pad Plated – Dia + .010” (254 $\mu$ )
- Minimum Capture Pad Filled – Dia + .006” (152.4 $\mu$ )
- Standard Via Spacing (Center To Center)  $\geq$  .020” (508 $\mu$ ) Dia
- Minimum Via Spacing (Edge to Edge) = 1 Dia.  $\geq$  .020”
- Minimum Via Spacing (To circuit edge) = 1 Dia.  $\geq$  .020”

**Solder Barriers**

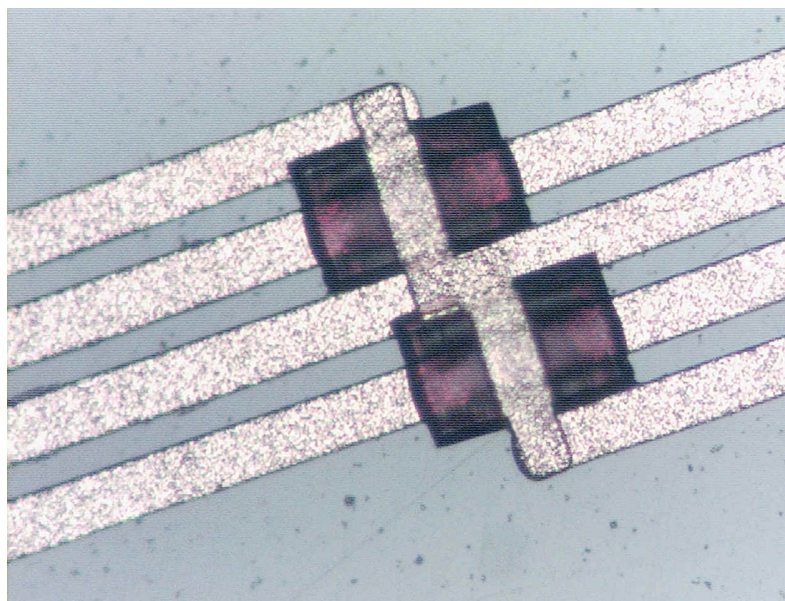
<b>Solder Barrier Parameters</b>			
	<b>Good</b>	<b>Better</b>	<b>Best</b>
	<b>Low-Temp Polymer</b>	<b>TiW</b>	<b>Ni Oxide</b>
Thickness	.0002" (5 $\mu$ )	.0002" (5 $\mu$ )	Defined in Metal Scheme
Maximum temperature	250°C = 60sec.	250°C = 60sec.	N/A
Minimum feature width	2.0 mils (50 $\mu$ )	2.0 mils (50 $\mu$ )	Full conductor width + 4 mils (101.6 $\mu$ )
Minimum gap	2.0 mils (50 $\mu$ )	2.0 mils (50 $\mu$ )	.004
Minimum conductor overlap onto ceramic or pullback	1.0 mils (25.4 $\mu$ )	1.0 mils (25.4 $\mu$ )	N/A
Minimum freestanding solder dam	N/A	N/A	N/A
Distance to circuit edge	3.0 mils (75 $\mu$ ) min	3.0 mils (75 $\mu$ ) min	N/A
Application side	-A or -B or both	-A or -B or both	-A or -B or both



**Cross-Over Bridges**



Cross-Over Bridge Design Rules		
Parameter	Minimum Value mils ( $\mu\text{m}$ )	Comment
Bridge Beam	1.0 (25)	
Bridge/Conductor Overlap	1 mil <sup>2</sup> ( $645\mu\text{m}^2$ )	
Bridge Length	3.0 (75)	Minimum
Insulator Dimension	1.5 (37.5) Length, 3.0 (75) Beam	
Encapsulation		Optional, factory quote only
Bridge Height	0.2 (5)	Minimum
Bridge Thickness	0.15 (3.8)	Minimum

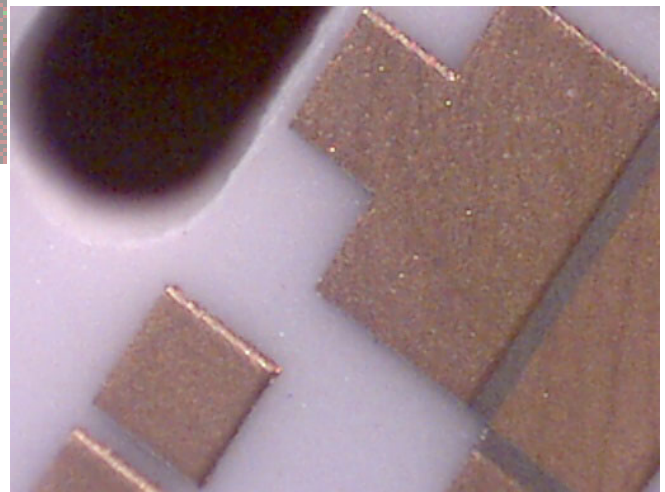
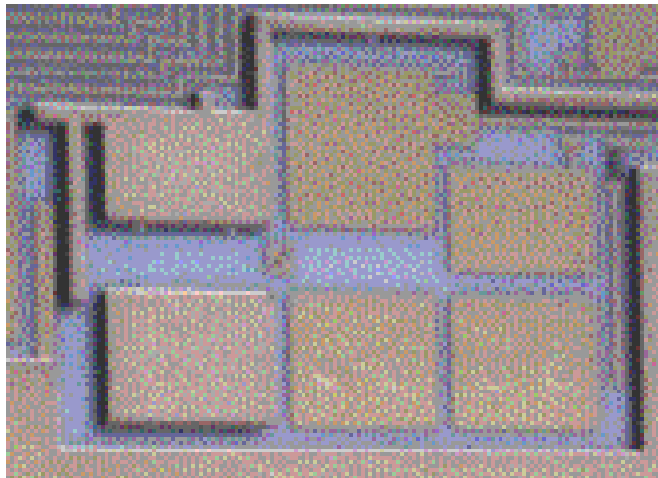


## High Conductivity Traces

Sheet Resistivities - Examples					
Metal	Thickness	Sputtered Sheet Resistance m ( $\Omega/\square$ )	Plated Sheet Resistance m ( $\Omega/\square$ )	Min Line Width	Tol. $\pm$
Au	80 $\mu\text{in}$ (2.03 $\mu\text{m}$ )	10-11	15-16	.0008"	.0001"
Au	150 $\mu\text{in}$ (3.81 $\mu\text{m}$ )	5-6	5-6	.0008"	.0001"
Au	600 $\mu\text{in}$ (15.24 $\mu\text{m}$ )	1.5	2.0	.002"	.0005"
Ni	20 $\mu\text{in}$ (0.5 $\mu\text{m}$ )	160	-	N/A	N/A
TiW	400 $\text{\AA}$	24,000	-	N/A	N/A
Cu	2000 $\mu\text{in}$ (50.8 $\mu\text{m}$ )	-	0.21	.004"	.001"

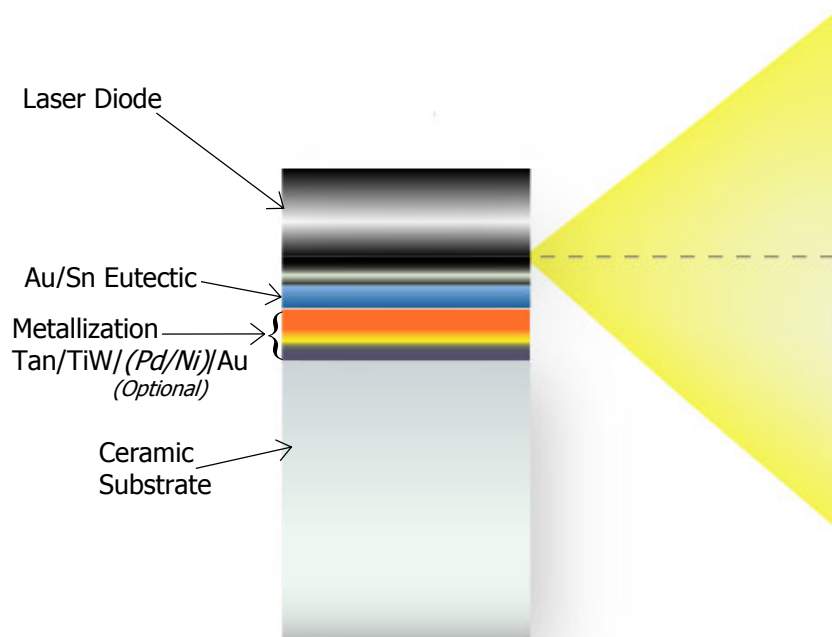
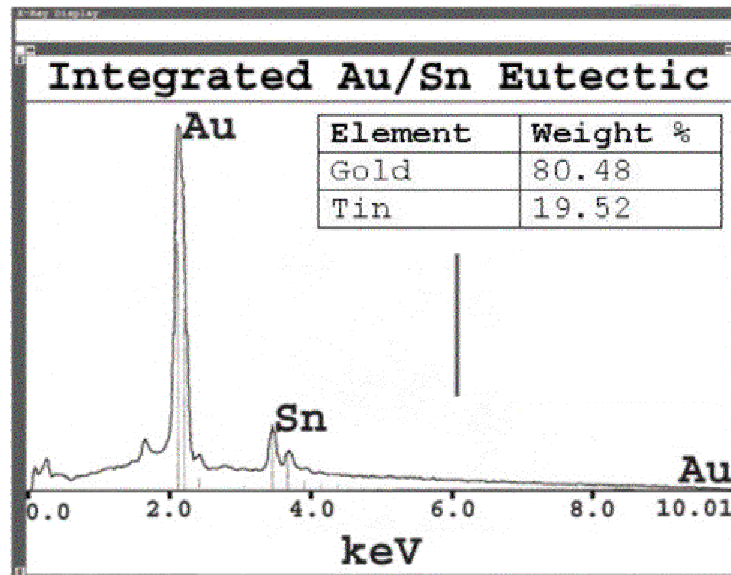
  

Typical Plating Thicknesses & Tolerances		
Plating Option	Metal	Thickness
Thick Copper	TiW	250-750 $\text{\AA}$ Sputtered
	Au	125 $\pm$ 25 $\mu\text{in}$ Sputtered or Plated
	Cu	2200 $\pm$ 400 $\mu\text{in}$ Plated
	Ni	80-250 $\mu\text{in}$ Plated
	Au	100-200 $\mu\text{in}$ Plated
Thick Au	TiW	250-750 $\text{\AA}$ Sputtered
	Au	400-1000 $\mu\text{in}$ Sputtered or Plated



### Integrated Eutectic

- Standard Thickness: 4 microns (.00016")
- Maximum Thickness: 8 Microns (.0003")
- Minimum Size: 127 Microns (5 mil square)
- Freeze Time: 120 seconds @ 320°C (Typical)



## Design Guidelines for Pre-Deposited Sputtered AuSn Eutectic Solder Pads

*Note: These guidelines are DITF's standard process capabilities. Tighter tolerances and/or dimensions may be provided, but must be discussed with DITF on an individual case basis.*

<b>AuSn Pad Properties</b>		
<b>Composition</b>	80% Au / 20% Sn Sputtered Eutectic	
<b>Melting Point</b>	284°C	
<b>Coefficient of Thermal Expansion</b>	16.5 ppm/°C	
<b>Thermal Conductivity</b>	58.6 W/mK	
<b>Freeze Time* (at 320°C)</b>	2 Minutes	
<b>Pre-Deposited AuSn Solder Pad Thickness (Max)</b>	8µm	320µin
<b>Minimum Pad Dimension</b>	>127µm	5 mils

*\*Note: The length of time that the solder holds the above conditions after it has reached 320°C.*

<b>Diablo Process Capabilities</b>			
<b>Dimension</b>	<b>(Metric)</b>	<b>Value</b>	<b>(English)</b>
Solder pad pullback from Au metallization, tight edge	>25 µm		>1 mil
Solder pad pullback from Au metallization, loose edge	>50 µm		>2 mils
Au metallization pullback from ceramic edge, tight edge	>25 µm		>1 mil
Au metallization pullback from ceramic edge, loose edge	>50 µm		>2 mils
AuSn pad gap	>50 µm		>2 mils

## Gold-Tin Deposition (Cross-Section)

<b>Dimension</b>	<b>(Metric)</b>	<b>Value</b>	<b>(English)</b>
Over etched area (estimated)	~0.50 µm		~0.02 mil
Chemically affected zone (estimated)	~12.7 µm		~0.50 mil
Recess of solder during reflow (estimated)	~0.50 µm		~0.02 mil
Solder pad feature tolerance	±25 µm		±1 mil
Solder pad placement tolerance	±25 µm		±1 mil
Minimum substrate thickness	252 µm		5.0 mils

## Calculating Minimum AuSn Pad Design Dimensions

The required AuSn solder pad dimensions are defined as the dimension of the nominal die or component to be mounted plus a tolerance factor ( $F_T$ ).

$$F_T = \text{SQRT}(X_1^2 + X_2^2 + X_3^2 + X_4^2 + X_5^2) + 2 * X_6$$

$$\text{Pad Dimension} = \text{Die/Component Dimension} + F_T$$

Aeroflex MIC Technology Defined Variables/Tolerances

	Dimension	Value	
$X_3$	Solder Pad Tolerance	~25 $\mu\text{m}$	~ 1.0 mil
$X_4$	Solder Reflow Recess (Estimated)	~0.5 $\mu\text{m}$	~0.02 mil
$X_5$	Over Etched Area (Estimated)	~0.5 $\mu\text{m}$	~0.02 mil
$X_6$	Chemically Affected Zone	~12.7 $\mu\text{m}$	~ 0.5 mil

Customer Defined Variables/Tolerances

	Dimension
$X_1$	Die/Component Tolerance
$X_2$	Die Attach Accuracy
$D_x$	Die/Component X Dimension
$D_y$	Die/Component Y Dimension

Sample Calculations – for a part with the following qualities. (units are metric)

Die Size – 508 $\mu\text{m}$  x 762  $\mu\text{m}$

Die Tolerance – 12 $\mu\text{m}$

Die Attach Accuracy – 25 $\mu\text{m}$

$$F_T = \text{SQRT}(X_1^2 + X_2^2 + X_3^2 + X_4^2 + X_5^2) + 2 * X_6$$

$$F_T = \text{SQRT}(12^2 + 25^2 + 25^2 + 0.5^2 + 0.5^2) + 2 * 12.7$$

$$F_T = 37.34 + 25.4$$

$$F_T = 62.8\mu\text{m}$$

$$\text{Pad Dimension (X)} = \text{Die/Component Dimension} + F_T$$

$$\text{Pad Dimension (X)} = 508 + 62.8 = 571 \mu\text{m}$$

$$\text{Pad Dimension (Y)} = \text{Die/Component Dimension} + F_T$$

$$\text{Pad Dimension (Y)} = 762 + 62.8 = 825 \mu\text{m}$$

$$\text{AuSn Pad Size} = 571 \mu\text{m} \times 825\mu\text{m}$$